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REMARKS

Claims 1-4, as amended, are presented for continued examination herein.

The following remarks are supplemental to the discussion presented in the Amendment Under 37 CFR §1.116 filed December 22, 2003.

Claims 1-4 have been amended more clearly to define the differences between the prior art of record and the applicant's invention.

Attention is directed to applicant's Fig. 2, showing lines 251 and 254 as input to three-input AND gate 210 and two-input AND gate 211. To detect a short circuit failure between any two terminals, appropriate logical values should be set for the other terminals. One of logical values "0" and "1" is set for input terminal A, while the other of the logical values is set for input terminal D. Then, to detect whether or not there is a possibility of a short circuit failure arising between lines 251 and 254 by an output terminal E of AND gate 210, input terminals B and C are set to a logical value "1" so that the logical value of output terminal E is changed by the logical value of input

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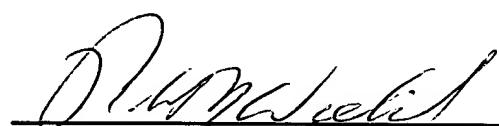
terminal A. Further, to detect the same by an output terminal F of a two-input AND gate 211, input terminal C is set to the logical value "1". Thus, a short circuit failure between any two adjacent terminals can be detected by setting the appropriate logical values of terminals other than the two adjacent terminals.

Prompt and favorable continued examination of this application on the merits is respectfully solicited.

Respectfully submitted,

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